Sub B1 Cont'd

24. (New) The method as recited in Claim 9 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the first and second openings, respectively.--

REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicant originally submitted Claims 1-20 in the application. The Applicant presently amends Claims 1-14, cancels Claims 15-20 without prejudice or disclaimer, and adds new Claims 21-24. Accordingly, Claims 1-14 and 21-24 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has objected to the specification as containing informalities; namely various typographical or grammatical errors. In response, the Applicant has amended the specification to correct these inadvertent errors and appreciates the Examiner's diligence in finding and bringing these errors to his attention.

II. Rejection of Claims 1, 2, 5, 7-9, 12, 14 and 15 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 5, 7-9, 12, 14 and 15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,262,041 to Gulla. However, Gulla fails to disclose a method of plating an electrical contact that includes forming first and second dielectric layers on

a metal interconnect over first and second sides of a printed wiring board, respectively, the first and second dielectric layers each having openings exposing portions of the metal interconnect, as recited in Claims 1 and 8 of the present application. Gulla also fails to disclose removing a portion of each of first and second plating layers from the first and second dielectric layers while leaving portions of the first and second plating layers under first and second contact layers, as recited in Claims 1 and 8.

In contrast, Gulla discloses forming a conductive coating 3 (used for plating) directly on a substrate 1 or, alternatively, forming a metal flash coat 7 (alternatively used for plating) directly on the conductive coating 3. (FIGs. 6 and 10; column 5, lines 9-24; column 8, lines 44-50). That is, in both embodiments disclosed in Gulla, the layer used for plating is either formed directly on the substrate 1 or is formed on the conductive coating 3 that is formed directly on the substrate 1, and is not formed on a dielectric layer because Gulla fails to even disclose a dielectric layer.

Therefore, Gulla does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 2, 5, 7, 9, 12, 14 and 15 are dependent upon Claims 1 and 8, Gulla also cannot be an anticipating reference for Claims 2, 5, 7, 9, 12, 14 and 15. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1, 2, 5, 7-9, 12, 14 and 15.

Gulla also does not anticipate new Claims 21-24 because these claims are also dependent on Claims 1 or 8.

III. Rejection of Claims 1, 6, 8 and 13 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 6, 8 and 13 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,162,365 to Bhatt, *et al.* ("Bhatt"). However, Bhatt fails to disclose a method of plating an electrical contact that includes forming first and second dielectric layers on a metal interconnect over first and second sides of a printed wiring board, respectively, the first and second dielectric layers each having openings exposing portions of the metal interconnect, as recited in Claims 1 and 8 of the present application. Bhatt also fails to disclose removing a portion of each of first and second plating layers from the first and second dielectric layers while leaving portions of the first and second plating layers under first and second contact layers, as recited in Claims 1 and 8. In contrast, Bhatt discloses forming a stack of conductive layers directly on a substrate 12, the stack consisting of a copper foil 14, a conductive metal layer 40, a noble metal layer 50 and a secondary finishing metal layer 70, and not including a dielectric layer. (Fig. 6; column 3, lines 1-5; column 3, line 65 through column 4, line 2; column 4, lines 7-9; column 4, lines 54-60).

Therefore, Bhatt does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 6 and 13 are dependent upon Claims 1 and 8, Bhatt also cannot be an anticipating reference for Claims 6 and 13. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1, 6, 8 and 13.

Bhatt also does not anticipate new Claims 21-24 because these claims are also dependent on Claims 1 or 8.

IV. Rejection of Claims 3, 4, 10 and 11 under 35 U.S.C. §103

The Examiner has rejected Claims 3, 4, 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Gulla in view of U.S. Patent No. 6,015,482 to Stern. However, as discussed above, Gulla fails to teach forming a plating layer on a dielectric layer, as required by Claims 1 and 8 of the present application. Gulla also fails to suggest forming a plating layer on a dielectric layer because Gulla fails to teach, suggest or even mention forming a dielectric layer, as discussed above.

Moreover, Stern adds nothing to Gulla because Stern also fails to teach or suggest forming a plating layer on a dielectric layer. In contrast, Stern merely teaches forming a stack of conductive layers on a substrate 12, the stack consisting of a copper foil 14, electroplated copper 20, a tin-nickel layer 22 and a gold layer 30, but not including a dielectric layer. (Fig. 2H; column 4, lines 45-52; column 5, lines 31-44; column 4 lines 55-57; column 6, lines 62-65). In fact, as with Gulla and Bhatt described above, Stern fails to even mention a dielectric layer.

Therefore, the combination of Gulla and Stern fails to teach or suggest the invention recited in independent Claims 1 and 8 and their dependent claims. Accordingly, the combination fails to support a *prima facie* case of obviousness of Claims 3, 4, 10 and 11. Claims 3, 4, 10 and 11 are therefore not obvious in view of the combination of Gulla and Stern

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 3, 4, 10 and 11 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

The combination of Gulla and Stern also fails to support a *prima facie* case of obviousness of Claims 21-24 because these claims are also dependent on Claims 1 or 8.

V. Additional References Made of Record

The Applicant believes that the additional references made of record and not relied upon by the Examiner are not as pertinent to the claimed invention as those relied on, but the Applicant retains the right to address these references in detail, if necessary, in the future.

VI. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-14 and 21-24.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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#5 attach

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

(1) Please amend the paragraph [0009] on page 5 as follows:

"[0009] In yet another aspect, the present invention provides[,] a substrate having dielectric layers located on opposing first and second sides of a substrate and having openings formed therein. The substrate further includes a [metalized] metallized via extending through the substrate and having a via metal extending therefrom where the openings contact the via metal. The substrate also has a discontinuous plating layer located within each of the openings and contacting the via metal. The substrate still further includes an electroplated contact layer located over each of the discontinuous plating layers where the electroplated contact layers are electrically connected to each other by the via metal."

(2) Please amend the paragraph [0021] on page 9 as follows:

"[0021] Referring initially to FIGURE 1, illustrated is a sectional view of a portion of one embodiment of an IC substrate 100 manufactured according to the principles of the present invention. FIGURE 1 illustrates [an A] a sectional view of a portion of the substrate 100 early in the manufacturing process, and includes a conventional printed wiring board (PWB) 110 as its core. The PWB 110 provides structural support for the overall substrate 100 and, in exemplary embodiments, the core may be composed of Bismaleimide Triazine (BT), fiberglass, copper or

other suitable, rigid material. Those skilled in the art understand the advantages associated with each of these materials, as well as other materials suitable for use as the core of the substrate 100."

(3) Please amend the paragraph [0027] on page 13 as follows:

"[0027] Referring now to FIGURE 4, illustrated is a sectional view of a portion of one embodiment of the substrate 100 after an etch resist 410 has been applied to the bottom side of the substrate 100. As shown in FIGURE 4, the etch resist 410 is applied in the lower openings 320 of the substrate 100 to protect the plating layer 150 on the second side of the substrate 100. An etchant is applied to the substrate 100 to perform a quick etch to remove the portions of the electro-less plating layers 150 exposed through the upper openings 310 and not protected by the etch resist 410. While the conductive layers 220 are exposed to the etch, the etch rate is slow enough such that the thinner plating layer 150 is removed while the thicker conductive layer 220 remains. The etch resist 410 prevents the previously exposed plating layer 150 on the second side from being etched away, thus allowing the plating layers 150 to maintain an electrical connection across the second side of the substrate 100, and to portions of the first side through the metal interconnect 130 and [Via] <u>via</u> 120."

(4) Please amend the title as follows:

<u>METHOD OF MANUFACTURING</u> A PRINTED WIRING BOARD HAVING A DISCONTINUOUS PLATING LAYER [AND METHOD OF MANUFACTURE THEREOF]

IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) A method of plating an electrical contact on a substrate, comprising:

forming a metal interconnect on first and second opposing sides of a printed wiring board and through a via formed through the printed wiring board;

forming first and second dielectric layers on the metal interconnect over the first and second sides of the printed wiring board, respectively, the first and second dielectric layers each having openings therethrough that expose portions of the metal interconnect;

forming [electrically connected] first and second plating layers on the first and second [opposing sides of a printed wiring board] dielectric layers, respectively, and in the first and second openings and on the exposed portions of the metal interconnect, the first and second plating layers electrically connected by the metal interconnect;

electroplating [a] first and second contact [layer] layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second [opposing sides] dielectric layers while leaving the portions of the first and second plating layers under the first and second contact [layer] layers.

(2) Please amend Claim 2 as follows:

2. (Amended) The method as recited in Claim 1 wherein forming [electrically connected] first and second plating layers includes forming the [electrically connected] first and second plating

layers with an electro-less process and the method further includes electroplating [a] first and second conductive [layer] layers on the first and second plating layers, respectively.

(3) Please amend Claim 3 as follows:

3. (Amended) The method as recited in Claim 1 wherein electroplating [a] first and second contact [layer] layers includes electroplating [a] first and second barrier [layer] layers over the first and second plating layers, respectively.

(4) Please amend Claim 4 as follows:

4. (Amended) The method as recited in Claim 3 wherein electroplating [a] first and second barrier [layer] layers includes electroplating [a] first and second nickel [layer] layers, respectively, and electroplating [a] first and second contact [layer] layers further includes electroplating [a] first and second gold [layer] layers on the first and second nickel [layer] layers, respectively.

(5) Please amend Claim 5 as follows:

5. (Amended) The method as recited in Claim 1 [further including forming a discontinuous conductive layer on each of the plating layers and] wherein forming the first plating layer[s] includes forming a discontinuous first plating layer [on the first side].

(6) Please amend Claim 6 as follows:

6. (Amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer [on the first side] prior to electroplating the first and second contact [layer] layers.

(7) Please amend Claim 7 as follows:

7. (Amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer [on the second side] subsequent to electroplating the first and second contact [layer] layers.

(8) Please amend Claim 8 as follows:

8. (Amended) A method of manufacturing an integrated circuit (IC) substrate, comprising:

forming a multi-layered substrate with a printed wiring board core and having [metalized] vias formed therethrough;

forming metal interconnects on first and second opposing sides of the printed wiring board and through the vias;

forming first and second dielectric layers on the metal interconnects over the first and second sides of the printed wiring board, respectively, the first and second dielectric layers each having openings therethrough that expose portions of the metal interconnects; and

plating an electrical contact on [a surface of] the substrate, including:

forming first and second plating layers on the first and second [opposing sides of the substrate] dielectric layers, respectively, and in the first and second openings and on the

exposed portions of the metal interconnects, the first and second plating layers electrically connected by one of the metal interconnects [and on a via metal extending from the via to thereby electrically connect the plating layers];

electroplating [a] first and second contact [layer] layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second [opposing sides] dielectric layers while leaving the portions of the first and second plating layers under the first and second contact [layer] layers.

(9) Please amend Claim 9 as follows:

9. (Amended) The method as recited in Claim 8 wherein forming [electrically connected] the first and second plating layers includes forming the [electrically connected] first and second plating layers with an electro-less process and the method further includes electroplating [a] first and second conductive [layer] layers on the first and second plating layers, respectively.

(10) Please amend Claim 10 as follows:

10. (Amended) The method as recited in Claim 8 wherein electroplating [a] first and second contact [layer] layers includes electroplating [a] first and second barrier [layer] layers over the first and second plating layers, respectively.

(11) Please amend Claim 11 as follows:

11. (Amended) The method as recited in Claim 10 wherein electroplating [a] first and second barrier [layer] layers includes electroplating [a] first and second nickel [layer] layers and electroplating [a] first and second contact [layer] layers further includes electroplating [a] first and second gold [layer] layers on the first and second nickel [layer] layers.

(12) Please amend Claim 12 as follows:

12. (Amended) The method as recited in Claim 8 [further including forming a discontinuous conductive layer on each of the plating layers and] wherein forming the first plating layer[s] includes forming a discontinuous first plating layer [on the first side].

(13) Please amend Claim 13 as follows:

13. (Amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer [on the first side] prior to electroplating the first and second contact [layer] layers.

(14) Please amend Claim 14 as follows:

14. (Amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer [on the second side] subsequent to electroplating the first and second contact [layer] layers.

(15) Please cancel Claim 15 without prejudice or disclaimer.

(16) Pursuant to the previous election of Claims 1-15 in response to a restriction requirement, please cancel Claims 16-20 without prejudice or disclaimer.

(17) Please add new Claims 21-24 as follows:

--21. (New) The method as recited in Claim 1 wherein the first and second plating layers are not formed in the via.

22. (New) The method as recited in Claim 2 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the first and second openings, respectively.

23. (New) The method as recited in Claim 8 wherein the first and second plating layers are not formed in the vias.

24. (New) The method as recited in Claim 9 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the first and second openings, respectively.--